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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/044,185
Filing Date: January 09, 2002
Appellant(s): KRAMER ET AL.

Steven J. Hanke
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 2/28/11 appealing from the Office action mailed 7/26/10.

**(1) Real Party in Interest**

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The following is a list of claims that are rejected and pending in the application:

Claims 1-20 are rejected.

**(4) Status of Amendments After Final**

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

**(5) Summary of Claimed Subject Matter**

The examiner has no comment on the summary of claimed subject matter contained in the brief.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

**(7) Claims Appendix**

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| US 2002/0110086 | Reches | 8-2002 |
| 5,412,648 | Fan | 5-1995 |
| US 6,975,638 B1 | Chen et al. | 12-2005 |
| 5,905,873 | Hartmann et al. | 5-1999 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 6-10, 13, and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Reches (U.S. Publication US 2002/0110086 A1) in view of Fan (U.S. Pat. 5412648).

**With respect to claims 1 and 8**, Reches discloses a non-blocking crossbar and method of operation **(See page 2 paragraph 24 of Reches for reference to a crossbar switch and a method for controlling the crossbar switch such that packets are not blocked by each other)**. Reches also discloses n inputs and n outputs **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the switch comprising N input ports and N output ports)**. Reches further discloses each of the outputs having a destination FIFO and n crossbar FIFOs wherein each of the n crossbar FIFOs interposes a corresponding one of each of said n inputs and the destination FIFO **(See page 4 paragraph 52, page 4 paragraph 55, and Figure 1 of Reches for reference to each output port having at least one output queue, which is an output FIFO, and for reference to input ports maintaining an output queue for each possible output port, meaning for each output port there are N queues corresponding to each of the N inputs and each of the queues are interposed**

**between a corresponding one of the N inputs and the destination FIFO)**. Reaches also discloses each of the n interposing crossbar FIFOs being unique to one of the n outputs **(See page 4 paragraph 55 and Figure 1 of Reches for reference to each of the output queues maintained by the input ports storing packets destined to each separate n output port, meaning each of these output queues is unique to a respective one of the n output ports)**. Reches also discloses a scheduler configured to cause a plurality of packets that are unencapsulated, unsegmented, and of differing lengths to be transmitted from one of the inputs toward one of the outputs when both the destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory to contain an entirety of a packet of the plurality of packets **(See page 1 paragraph 8, page 4 paragraph 56 to page 5 paragraph 59, and Figure 1 of Reches for reference to forwarding variable length packets that are not segmented or encapsulated and for reference to a scheduler 40 that causes packets to be sent from an input to an output only when it is determined that there is sufficient memory and resources to send the entire packet in a set of time slots where the packet will not be blocked by other packets currently being sent)**. Reches does not specifically disclose causing packets to be transmitted only when a destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory at the same time to receive and then contain an entirety of the packets.

**With respect to claims 1 and 8**, Fan, in the field of communications, discloses scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive

and then contain an entirety of a packet **(See the abstract, column 3 line 37 to column 4 line 39 and Figure 1 of Fan for reference FIFOs having counters to count the amount of idle space available in the FIFOs and reporting the amount of available space such that packets are sent from an input a destination FIFO only when the FIFOs have a sufficient amount of idle space for accepting an entire cell)**. Scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet has the advantage of allowing packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Fan, to combine scheduling packets to be transmitted only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets, as suggested by Fan, with the system and method of Reches, with the motivation being to allow packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

**With respect to claims 2 and 9**, Reches discloses that the scheduler is further configured to select one of the inputs based upon a priority thereof **(See page 2 paragraph 18 of Reches for reference to forwarding packets from selected source ports based on priority level of the source port)**.

**With respect to claims 3 and 10**, Reches discloses that the scheduler is further configured to select one of the outputs based upon a priority thereof **(See page 4 paragraph 52 for reference to scheduler 40 forwarding packets to output ports based on output port queue priority levels)**.

**With respect to claims 6 and 13**, Reches discloses each output comprising an output arbiter configured to select one of the crossbar FIFOs and transfer a packet therein to the destination FIFO **(See page 4 paragraph 52 and page 5 paragraph 58 for reference to each output port having an arbiter that uses an arbitration scheme to transfer packets from input queues to output queues)**.

**With respect to claims 7 and 14**, Reches discloses that the arbiter is further configured to select one of the crossbar FIFOs based upon packet priority **(See page 3 paragraph 36 of Reches for reference to selecting packets to be transferred from input queues to output queues based on the priority of the packet)**.

3. Claims 4, 5, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Fan and in further view of Chen et al. (U.S. Pat. 6975638 B1).

**With respect to claims 4, 5, 11, and 12**, the combination of Reches and Fan does not specifically disclose that at least two of the n inputs are coupled to different types of packet based fabrics with the inputs and outputs being connected to a SONET network and two Ethernet networks.

**With respect to claims 4, 5, 11, and 12**, Chen et al. discloses a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network **(See column 5 lines 7-18 and Figure 3 of Chen et al. for reference to a crossbar switching having inputs connected to Gigabit Ethernet networks and a SONET network)**. A crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network has the advantage of allowing the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Chen et al., to combine a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network, as suggested by Chen et al., with the system and method of Reches and Fan., with the motivation being to allow the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

4. Claims 15-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Fan and in further view of Hartmann et al. (U.S. Pat. 5905873).

**With respect to claim 15**, Reches discloses a multi-channel network line card for packet based networks **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to a switch having input ports that correspond to a line multi-channel network line card)**. Reches also discloses n physical interfaces and inputs numbering at least three **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the switch comprising N input ports, which are physical interfaces, numbering**

**at least three)**. Reches further discloses a non-blocking crossbar coupled to the physical interfaces **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to a configurable switch unit 50, which corresponds to a non-blocking crossbar coupled to the input ports)**. Reches also discloses n outputs that transmit the packet to corresponding ones of the n physical interfaces **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the switch comprising N output ports transmitting packets to physical interfaces)**. Reches further discloses each of the outputs having a destination FIFO and n crossbar FIFOs wherein each of the n crossbar FIFOs interposes a corresponding one of each of the n inputs and the destination FIFO **(See page 4 paragraph 52, page 4 paragraph 55, and Figure 1 of Reches for reference to each output port having at least one output queue, which is an output FIFO, and for reference to input ports maintaining an output queue for each possible output port, meaning for each output port there are N queues corresponding to each of the N inputs and each of the queues are interposed between a corresponding one of the N inputs and the destination FIFOs**. Reaches also discloses each of the n interposing crossbar FIFOs being unique to one of the n outputs **(See page 4 paragraph 55 and Figure 1 of Reches for reference to each of the output queues maintained by the input ports storing packets destined to each separate n output port, meaning each of these output queues is unique to a respective one of the n output ports)**. Reches also discloses a scheduler configured to cause a plurality of packets that are unencapsulated, unsegmented, and of differing lengths to be transmitted from one of the inputs toward one of the outputs when both

the destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory to contain an entirety of a packet of the plurality of packets **(See page 1 paragraph 8, page 4 paragraph 56 to page 5 paragraph 59, and Figure 1 of Reches for reference to forwarding variable length packets that are not segmented or encapsulated and for reference to a scheduler 40 that causes packets to be sent from an input to an output only when it is determined that there is sufficient memory and resources to send the entire packet in a set of time slots where the packet will not be blocked by other packets currently being sent)**. Reches does not specifically disclose causing packets to be transmitted only when a destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory at the same time to receive and then contain an entirety of the packets. Reches also does not specifically disclose n network processors that convert a packet between protocols coupled to corresponding ones of the n physical interfaces.

**With respect to claim 15**, Fan, in the field of communications, discloses scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet **(See the abstract, column 3 line 37 to column 4 line 39 and Figure 1 of Fan for reference FIFOs having counters to count the amount of idle space available in the FIFOs and reporting the amount of available space such that packets are sent from an input a destination FIFO only when the FIFOs have a sufficient amount of idle space for accepting an entire cell)**. Scheduling packets to be transmitted through a switch only when a destination

FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet has the advantage of allowing packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Fan., to combine scheduling packets to be transmitted only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets, as suggested by Fan, with the system and method of Reches, with the motivation being to allow packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

**With respect to claim 16**, Reches discloses a fast pattern processor that receives a packet from a physical interface and analyzes and classifies the packet **(See page 3 paragraph 36 of Reches for reference to an input port receiving a packet and analyzing the packet to determine parameters including the priority of the packet, which is a classification of the packet)**. Reches does not disclose processing the packet and converting the packet into an appropriate network protocol.

**With respect to claims 15 and 16**, Hartmann et al., in the field of communications, discloses network processors coupled to corresponding physical interfaces that convert received packets between protocols **(See the abstract of Hartmann et al. for reference to port adaptors, which are network processors,**

**coupled to input ports, which are physical interfaces, that receive packets and convert them between different types of communication formats, which are protocols)**. Using network processors coupled to corresponding physical interfaces that convert received packets between protocols has the advantage of allowing all packets being sent through a crossbar switch to have a common protocol, such that it is easier to switch the packets **(See the abstract of Hartmann et al. for reference to this advantage)**.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Hartmann et al., to combine using network processors coupled to corresponding physical interfaces that convert received packets between protocols, as suggested by Hartmann et al., with the system and method of Reches and Fan, with the motivation being to allow all packets being sent through a crossbar switch to have a common protocol, such that it is easier to switch the packets.

**With respect to claim 17**, Reches discloses that the scheduler is further configured to select one of the inputs based upon a priority thereof **(See page 2 paragraph 18 of Reches for reference to forwarding packets from selected source ports based on priority level of the source port). Reches also discloses that the scheduler is further configured to select one of the outputs based upon a priority thereof (See page 4 paragraph 52 for reference to scheduler 40 forwarding packets to output ports based on output port queue priority levels)**.

**With respect to claim 20**, Reches discloses each output comprising an output arbiter configured to select one of the crossbar FIFOs and transfer a packet therein to

the destination FIFO **(See page 4 paragraph 52 and page 5 paragraph 58 for reference to each output port having an arbiter that uses an arbitration scheme to transfer packets from input queues to output queues)**. Reches discloses that the arbiter is further configured to select one of the crossbar FIFOs based upon packet priority **(See page 3 paragraph 36 of Reches for reference to selecting packets to be transferred from input queues to output queues based on the priority of the packet)**.

5. Claims 18 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Fan and Hartmann et al. and in further view of Chen et al.

**With respect to claims 18 and 19**, the combination of Reches, Fan, and Hartmann et al. does not specifically disclose that at least two of the n inputs are coupled to different types of packet based networks with the inputs and outputs being connected to a SONET network and two Ethernet networks.

**With respect to claims 18 and 19**, Chen et al. discloses a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network **(See column 5 lines 7-18 and Figure 3 of Chen et al. for reference to a crossbar switching having inputs connected to Gigabit Ethernet networks and a SONET network)**. A crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network has the advantage of allowing the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Chen et al., to combine a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network, as suggested by Chen et al., with the system and method of Reches, Fan, and Hartmann et al., with the motivation being to allow the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

**(10) Response to Argument**

Regarding Applicant's argument that Reaches does not teach a non-blocking crossbar comprising n output where each of the n outputs has a destination FIFO and n crossbar FIFOs, the Examiner respectfully disagrees. Applicant argues that the language of claim 1 requires the claimed crossbar FIFOs to be "in the output" (See the arguments on pages 6-8 of the Appeal Brief); however, the Examiner disagrees with this interpretation of the claim language. Claim 1 includes a limitation stating "n outputs, each of said outputs having a destination first-in, first-out buffer (FIFO) and n crossbar FIFOs". Thus, the claim language requires the n outputs to "have" n crossbar FIFOs; however, the use of word "having" does not require that the crossbar FIFOs be "in" the outputs, as argued by the Applicant. The word "have" has many meanings including "to posses, "to own", "to hold for use", etc. Using the broadest reasonable interpretation of the claim language the phrase "each of said outputs having... n crossbar FIFOs" may be interpreted to mean that each of the outputs "owns" or "holds for use" n crossbar FIFOs.

Therefore it is not clear that the claim language limits the crossbar FIFOs to being "in the output" as argued by the Applicant.

Next, as shown in the Response to Arguments section of the Final Rejection mailed 7/26/10, Reches discloses a switch having n inputs, n outputs, and n crossbar FIFOs of each the n outputs with each of the n crossbar FIFOs interposing a corresponding one of each of said n inputs and a destination FIFO (See page 4 paragraph 52, page 4 paragraph 55, and Figure 1 of Reches for reference to a switch having n inputs, n outputs, and n queues Q, which are crossbar FIFOs, of each of the n outputs with each of the n queues Q interposing a corresponding one of each of the n inputs and an output queue). Further, each of the queues is uniquely assigned to and thus "owned" by a single specific output. The queues Q of Reches are each indexed by an ordered pair Q(x,y) wherein x refers to an input corresponding to the queue and y refers to an output corresponding to the queue. For example, Figure 2 of Reches shows that output 1 has corresponding queues Q(1,1),... Q(M,1),… and Q(N,1), wherein Q(1,1) interposes input 1 and the output queue of output 1, wherein Q(M,1) interposes input M and the output queue of output 1, and wherein Q(N,1) interposes input N and the output queue of output 1. Thus, each output of Reaches has 1-N corresponding queues Q equivalent to the claimed n crossbar FIFOs. Therefore, Reaches does disclose n outputs, each of said outputs having a destination first-in, first-out buffer (FIFO) and n crossbar FIFOs, as claimed.

Further, even if the language of claim 1 were amended to explicitly state that the crossbar FIFOs were "in the output", it is still believed that such a limitation would be

obvious in view of the teachings of Reaches. Labeling the elements of a crossbar switch to be included in an input or in an output does not provide any limitations regarding the physical and structural relationship between these elements. For example, Applicant's own Figure 2 shows a block diagram of a non-blocking crossbar. It is clear from Figure 2 that the physical outputs (output 1, output 2, and output 3) are different from the physical destination FIFOs and the physical crossbar FIFOs. Labeling the destination FIFOs and the physical crossbar FIFOs as being included in the outputs is merely a logical labeling of the physical elements and does not change their physical location in relation to each other. Reaches discloses a switch having elements corresponding to the claimed inputs, outputs, destination FIFOs, and crossbar FIFOs (See page 4 paragraph 52, page 4 paragraph 55, and Figure 1 of Reches for reference to the inputs, outputs, output queues, and queues Q of Reaches). The physical location of each of the inputs, outputs, output queues, and queues Q of Reaches with respect to each other is the same in Figure 1 of Reaches as the corresponding elements of the Applicant's Figure 2. Therefore, the physical structure of the elements claimed crossbar and the switch of Reaches are identical. Logically drawing a box around specific physical elements and labeling them as part of the output does not change the physical structure of the crossbar. Therefore, even if the language of claim 1 were amended to explicitly state that the crossbar FIFOs were "in the output", it is believed that it is an obvious variation for one of ordinary skill in the art at the time of the invention to re-label the elements of Reaches such that the queues Q of Reaches are considered part of the

output of Reaches, since the switch of Reaches has the same physical components located in the same locations as the claimed crossbar.

The table below is used to provide a further comparison between language of claim 1, Figure 2 of the Applicant's specification, and Figure 1 of Reches.

| CLAIM 1 LANGUAGE | APPLICANT'S FIGURE 2 | RECHES FIGURE 1 |
|---|---|---|
| n inputs | input 1, input 2, and input 3; wherein n=3 | inputs 1-N |
| n outputs | output 1, output 2, and output 3; wherein n=3 | outputs 1-N |
| each output having a destination FIFO | destination FIFO 216 of output 1, destination FIFO 226 of output 2, and destination FIFO 236 of output 3 | each output having an output queue (See page 4 paragraph 52) |
| n crossbar FIFOs interposing a corresponding one of each of the n inputs and said destination FIFO | crossbar FIFOs 210, 212, and 214 respectively between corresponding inputs 1, 2, and 3, and destination FIFO 216 | Queues Q(1,1), Q(M,1), and Q(N,1) respectively between corresponding inputs 1, M, and N and the output queue of output 1 |

Applicant's arguments directed towards claim 8 (see page 8 of the Appeal Brief), claim 15, (see pages 8-9 of the Appeal Brief), claims 2, 3, 6, 7, 9, 10, 13, and 14 (see

page 9 of the Appeal Brief), claims 4, 5, 11, and 12 (see page 10 of the Appeal Brief), claims 16, 17, and 20, (See page 11 of the Appeal Brief), and claims 18 and 19 (see page 10 of the Appeal Brief) merely reference same arguments directed towards claim 1 and do not provide any further specific arguments. Therefore, it is believed that these claims are rendered obvious in view of the prior art for the same reasons discussed for claim 1 above.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Jason Mattis

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